REMARKS

By this amendment, Applicants' have cancelled claim 8 and amended claims 5, 6 and 7.

The Examiner has rejected claims 5-8 under 35 U.S.C. 102(b) as being anticipated by Kim (U.S. Patent No. 5,880,612).

With respect to claim 5, Kim discloses, in Fig. 2, a circuit and its corresponding jitter inducing method comprising the steps of a) setting delay times [232] for rising and/or falling edges of pulses in a reference pulse train [234] for sequential interval of the reference pulse train, and b) providing pulses of the reference pulse train [234] in order of the corresponding intervals wherein delays are applied to the rising ans/or falling edges of the pulses by said delay time [232] being set every interval.

With respect to claim 6, Kin discloses, in Fig. 2, that the changes of the delay time over the intervals are a function of a delayed time transition waveform [216/218].

With respect to claim 7, Kin discloses, in Fig. 2, a circuit and its corresponding pulse generating method for providing a pulse train derived from a reference pulse train [234] divided into sequential intervals wherein delay times [232] applied to rising and/or falling edges of pulses in the reference pulse train are set interval by interval, and the changes of the delay times over the sequential intervals are controlled to be a desired function.

With respect to claim 8, Kim discloses, in Fig. 2, that the delay times [232] are controlled according to the desired function determined by parameters designated through a user interface [MAX DELAY SELECT].

The Examiner has allowed claims 1-4 and 9-12.

The following statement of reasons for the indication of allowable subject matter:

The closest prior are of record does not show or fairly suggest:

a) A jitter inducing circuit including a switch control means for controlling a switch means to provide pulses to one delay means in which a setup of a delay time has finished, as called for in claim 1;

b) A jitter inducing method including steps of switching the supply of a reference pulse train to a second delay block from a first delay block and delaying the reference pulse train by the second delay block and providing an output to an output terminal, as called for in claim 9;

c) A circuit for generating a pulse train, in which a pulse providing means for providing a pulse to be jittered and a pulse not to be jittered to separate delay blocks of a plurality of delay blocks wherein both pulses are derived from a reference pulse train, and the delay times for the delay block to which the non-jittered pulse is provided is fixed, and

the delay time of the delay block to which the pulse to be jittered is provided changes sequentially, as called for in claim 11; and

d) A pulse generating method including the steps of (a) delaying rising edge or falling edge of a pulse to be jittered according to a preset delay time and (b) composing a non-jittered pulse and the pulse delayed in step (a) as called for in claim 12.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Iwasa et al. (U.S. Patent No. 5,327,411) discloses a write control method in a circuit having a first delay and a second delay and a control signal generating circuit.

Prior art Kaplinshy (U.S. Patent No. 5, 298,866) discloses a clock distribution circuit with active de-skewing.

Claim 5 of Applicants' invention recites a jitter inducing method wherein delay times are set for rising and/or falling edges of pulses in a reference pulse train for sequential intervals of the reference pulse train with changes of the delay times over the sequential intervals controlled to be a desired function determined by parameters designated through a user interface. The pulses of the reference pulse train are provided in order of the corresponding intervals wherein delays are applied to the rising and/or falling edges of the pulses by the delay times being set every interval. The delay times applied to rising and/or falling edges of pulses in the reference pulse train may be set interval by interval with the changes of the delay times over the intervals being a function of a delayed time transition waveform.

The Examiner asserts that claims 5-8 are anticipated by Kim (U.S. Patent No. 5,880,612) by equating the setting of the delay times in Applicants' claimed invention to the MAX_DELAY_SELECT signal applied to the delay lines A and B via bus 232. Kim teaches that the MAX_DELAY_SELECT signal is a two-bit digital words applied to a partial 2:4 decoder 602 which generates select signals SEL1, SEL12 and SEL123. The select signals are applied to various transistors in the DELAY LINES A and B for coupling selected delay groups into the DELAY LINES A and B. Each delay group includes multiple delay blocks that receive a control signal from one of the CHARGE PUMPS A and B. The control signal varies the resistance of transistors in the delay blocks to vary the delay of the delay blocks and hence the DELAY LINES A and B. The Kim states at column 6, lines 15-19: "The maximum select delay determines the greatest amount of timing skew which may be counter-adjusted by the dual delay-locked loop 200, and affords use of the dual delay-locked loop 200 for signals within a wide frequency range." Kim further states at Column 8, lines 25-27: "For each possible selected maximum delay, a variable delay is afforded within a range not exceeding the selected maximum delay. The teaching of Kim clearly identifies

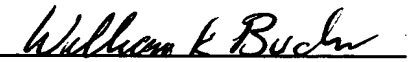
the MAX_DELAY_SELECT signal as selecting the maximum delay for the DELAY LINES A and B.

In contradistinction, Applicants' claim 5 recites the setting of setting delay times for rising and/or falling edges of pulses in a reference pulse train for sequential intervals of the reference pulse train wherein changes of said delay times over the sequential intervals are controlled to be a desired function determined by parameters designated through a user interface. The MAX_DELAY_SELECT signal of Kim does not control changes of the delay times over the sequential intervals of the reference pulse train to be a desired function determined by parameters designated through a user interface. The MAX_DELAY_SELECT signal of Kim only sets the maximum delay possible for the DELAY LINES A and B by coupling more or less delay groups into the DELAY LINES A and B.

In view of the cancellation of claim 8 and the amendments to claims 5, 6, and 7, Applicants respectfully request that the Examiner withdraw the rejections of the claims and pass this case to issue.

In accordance with current Patent Office practice, the Examiner is expressly authorized to call the undersigned agent at the number listed below if it is deemed the application is in other than condition for allowance or if prosecution can be expedited.

Respectfully submitted,

By 

William K. Bucher
Reg. No. 32,686
Patent Agent for Applicants

TEKTRONIX, INC.
P. O. Box 500 (50-LAW)
Beaverton, OR 97077
Phone (503) 627-7267 or (800) 835-9433
Attorney Docket No. 7465-US1

July 7, 2005